| S.No | VLSI (IEEE 2016-17) |
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| 1 | Designing Low Power and Durable Digital Blocks Using Shadow Nano electromechanical Relays |
| 2 | Corrections to “A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones” |
| 3 | A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting |
| 4 | One Minimum Only Trellis Decoder for Non-Binary Low-Density Parity-Check Codes |
| 5 | High-Throughput LDPC-Decoder Architecture Using Efficient Comparison Techniques & Dynamic Multi-Frame Processing Schedule |
| 6 | An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC |
| 7 | Circuit and Architectural Co-Design for Reliable Adder Cells With Steep Slope Tunnel Transistors for Energy Efficient Computing. |
| 8 | VLSI Implementation of Fully Parallel LTE Turbo Decoders. |
| 9 | An Efficient VLSI Architecture for Discrete Hadamard Transform. |
| 10 | Fast Kalman-Like Optimal Unbiased FIR Filtering With Applications |
| 11 | FIR Filter Design by Convex Optimization Using Directed Iterative Rank Refinement Algorithm |
| 12 | Implementation of digital filters in the residue number system |

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| 13 | VLSI Implementation of Fully Parallel LTE Turbo Decoders |
| 14 | Design and FPGA Implementation of Reconfigurable Linear-Phase Digital Filter With Wide Cutoff Frequency Range and Narrow Transition Bandwidth |
| 15 | On the Total Power Capacity of Regular-LDPC Codes With Iterative Message-Passing Decoders |
| 16 | A Relaxed Min-Sum LDPC Decoder With Simplified Check Nodes |
| 17 | An Efficient Decoder Architecture for Non binary LDPC Codes with Extended Min-Sum Algorithm |
| 18 | A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic |
| 19 | An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code |
| 20 | Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding |
| 21 | Algorithm and Architecture of Configurable Joint Detection and Decoding for MIMO Wireless Communications With Convolutional Codes |
| 22 | A Low-Cost, Radiation-Hardened Method for Pipeline Protection in Microprocessors |
| 23 | Design for Testability of Sleep Convention Logic |
| 24 | Temperature and Voltage Measurement for Field Test Using an Aging-Tolerant Monitor. |
| 25 | Area-Delay Efficient Digit-Serial Multiplier Based on k-Partitioning Scheme Combined With TMVP Block Recombination Approach |
| 26 | Low-Power/Cost RNS Comparison via Partitioning the Dynamic Range |
| 27 | A Fully-Integrated Digital LDO with Coarse-Fine-Tuning and Burst-Mode Operation |

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| 28 | A Multimode Area-Efficient SCL Polar Decoder |
| 29 | An Efficient Decoder Architecture for Non binary LDPC Codes with Extended Min-Sum Algorithm |
| 30 | Energy and Area Efficient Three-Input XOR/XNORs With Systematic Cell Design Methodology |
| 31 | Efficient Implementation of Scan Register Insertion on Integer Arithmetic Cores for FPGAs |
| 32 | A Novel Quantum-Dot Cellular Automata -bit -bit SRAM |
| 33 | High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels |
| 34 | Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication |
| 35 | Characterization of a Novel Low Leakage Power and Area Efficient 7T SRAM Cell |
| 36 | A Robust Energy/Area-Efficient Forwarded-Clock Receiver With All-Digital Clock and Data Recovery in 28-nm CMOS for High-Density Interconnects |
| 37 | A Hybrid Energy Efficient Digital Comparator |
| 38 | A Novel Thyristor-Based Silicon Physical Unclonable Function |
| 39 | A Comparator-Based Rail Clamp . |
| 40 | A 1-GS/s 9-bit Zero-Crossing-Based Pipeline ADC Using a Resistor as a Current Source. |
| 41 | All-Digital Duty-Cycle Corrector With a Wide Duty Correction Range for DRAM Applications |
| 42 | Low-Power/Cost RNS Comparison via Partitioning the Dynamic Range. |
| 43 | Analytical design optimization of sub-ranging ADC based on stochastic comparator. |
| 44 | In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers |
| 45 | A Low-Cost, Radiation-Hardened Method for Pipeline Protection in Microprocessors |
| 46 | Design Methodology for Voltage-Scaled Clock Distribution Networks. |
| 47 | Efficient Implementation of Scan Register Insertion on Integer Arithmetic Cores for FPGAs |

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| 48 | A Low-Power High-Performance Single-Cycle Tree-Based 64-Bit Binary Comparator FPGAs |
| 49 | A 167-ps 2.34-mW Single-Cycle 64-Bit Binary Tree Comparator With Constant-Delay Logic in 65-nm CMOS. |
| 50 | One-Cycle Correction of Timing Errors in Pipelines With Standard Clocked Elements. |
| 51 | Reducing Power, Leakage, and Area of Standard-Cell ASICs Using Threshold Logic Flip-Flops. |
| 52 | A Fast-Acquisition All-Digital Delay-Locked Loop Using a Starting-Bit Prediction Algorithm for the Successive-Approximation Register. |
| 53 | An Improved Design of a Reversible Fault Tolerant LUT-based FPGA.. |
| 54 | TCAD-Assisted Capacitance Extraction of Fin FET SRAM and Logic Arrays. |
| 55 | An Efficient Decoder Architecture for Non binary LDPC Codes with Extended Min-Sum Algorithm |
| 56 | High-Performance NB-LDPC Decoder With Reduction of Message Exchange |
| 57 | Reduced-Complexity Non binary LDPC Decoder for High-Order Galois Fields Based on Trellis Min-Max Algorithm |
| 58 | Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology |
| 59 | Register-Less NULL Convention Logic |
| 60 | A novel low-cost dynamic logic reconfigurable structure strategy for low power optimization |
| 61 | Optimum pMOS-to-nMOS Width Ratio for Efficient Sub threshold CMOS Circuits |
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| 64 | High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels |
| 65 | Multiple Constant Multiplication Algorithm for High-Speed and Low-Power Design |

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| 66 | Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation |
| 67 | Low Complexity Multi ternary Digit Multiplier Design in CNTFET Technology |
| 68 | Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation |
| 69 | An Efficient Hardware Implementation of Canny Edge Detection Algorithm |
| 70 | Built-in Self-Heating Thermal Testing of FPGAs |
| 71 | A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications |
| 72 | High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels |
| 73 | Implementation of a PID control PWM Module on Altera DE0 Kit Using FPGA |
| 74 | Distributed Sensor Network-on-Chip for Performance Optimization of Soft-Error-Tolerant Multiprocessor System-on-Chip |
| 75 | A Low-cost and Modular Receiver for MIMO SDR |
| 76 | VLSI Realization of a Secure Cryptosystem for Image Encryption and Decryption |
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